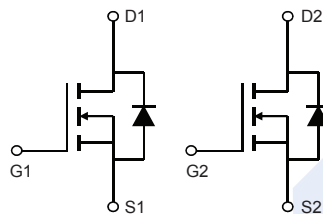
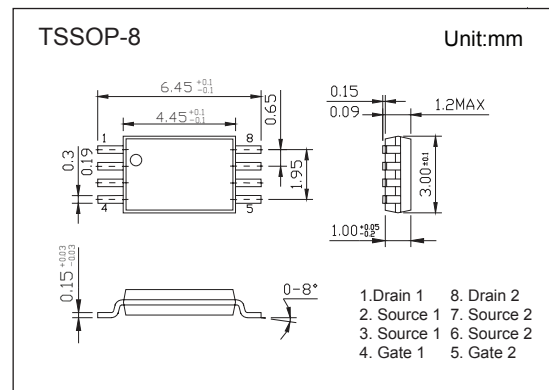


Dual N-channel MOSFET

2KK7103

■ Features

- $V_{DS} = 20V$
- $I_D = 6 A$
- $R_{DS(on)} \leq 30m\Omega$ ($V_{GS}=4.5V$)
- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance



■ Absolute Maximum Ratings ($T_a = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current	I_D	6	A
Pulsed Drain Current	I_{DM}	30	
Continuous Source Current (Diode Conduction) ^{a,b}	I_S	1.7	
Power Dissipation	P_D	$T_a = 25^\circ C$	W
		$T_a = 100^\circ C$	
Thermal Resistance, Junction- to-Case	$R_{\theta JC}$	30	$^\circ C/W$
Thermal Resistance, Junction- to-Ambient (PCB mounted)	$R_{\theta JA}$	62.5	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$

Notes:

- Pulse width limited by the Maximum junction temperature
- Surface Mounted on FR4 Board, $t \leq 5$ sec.

Dual N-channel MOSFET

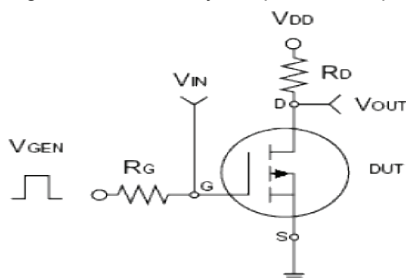
2KK7103

■ Electrical Characteristics ($T_a = 25^\circ\text{C}$, unless otherwise specified)

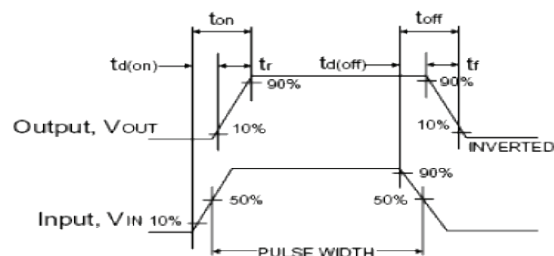
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DSS}	$I_D=250\mu\text{ A}$, $V_{GS}=0\text{V}$	20			V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20\text{V}$, $V_{GS}=0\text{V}$			1	$\mu\text{ A}$	
Gate-Body Leakage Current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 12\text{V}$			± 100	nA	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{ A}$	0.6		2	V	
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 4.5\text{V}$, $I_D = 6.0\text{A}$			30	m Ω	
		$V_{GS} = 2.5\text{V}$, $I_D = 5.2\text{A}$			40		
On-State Drain Current ^a	$I_{D(ON)}$	$V_{DS} = 5\text{V}$, $V_{GS} = 4.5\text{V}$	30			A	
Dynamic ^b							
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}$, $V_{DS}=8\text{V}$, $f=1\text{MHz}$		565		pF	
Output Capacitance	C_{oss}			105			
Reverse Transfer Capacitance	C_{rss}			75			
Total Gate Charge	Q_g	$V_{DS}=10\text{V}$, $I_D=6\text{A}$, $V_{GS}=4.5\text{V}$		5		nC	
Gate Source Charge	Q_{gs}			1			
Gate Drain Charge	Q_{gd}			1.5			
Switching ^c							
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{V}$, $R_L = 10\Omega$, $I_D = 1\text{A}$, $V_{GEN} = 4.5\text{V}$, $R_G = 6\Omega$		8	20	ns	
Turn-On Rise Time	t_r				10		20
Turn-Off Delay Time	$t_{d(off)}$				22		45
Turn-Off Fall Time	t_f				6		15

Notes:

- pulse test: $PW \leq 300\mu\text{ s}$, duty cycle $\leq 2\%$
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.



Switching Test Circuit



Switchin Waveforms

■ Marking

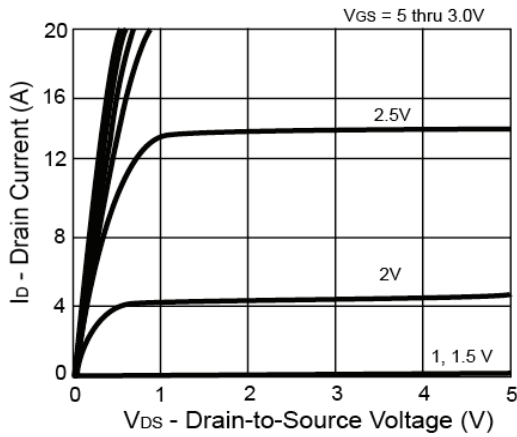
Marking	K7103 KA****
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Dual N-channel MOSFET

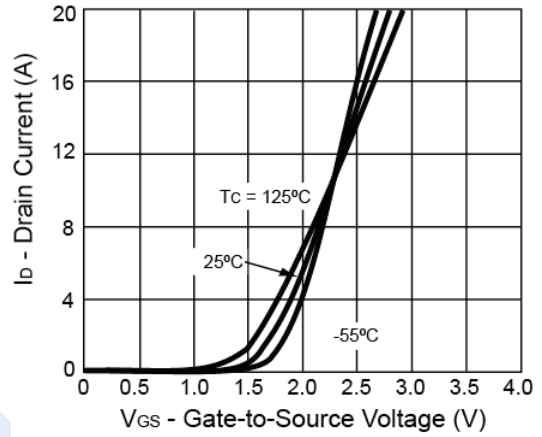
2KK7103

Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

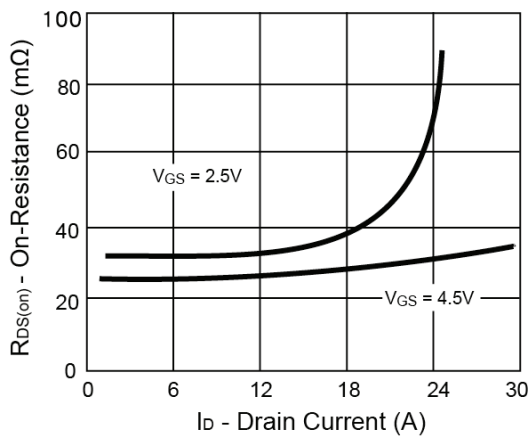
Output Characteristics



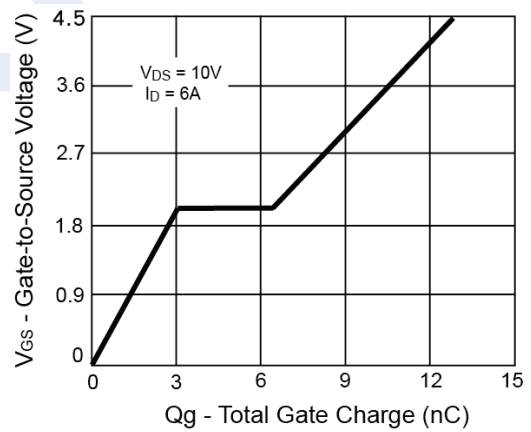
Transfer Characteristics



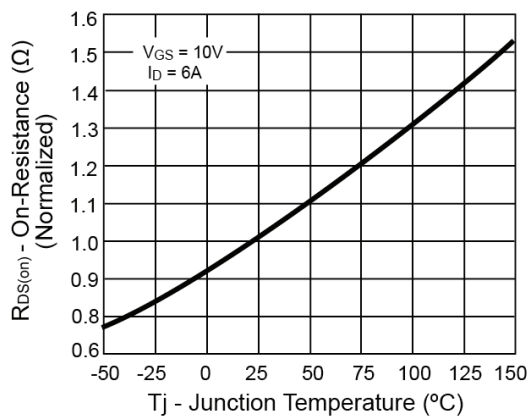
On-Resistance vs. Drain Current



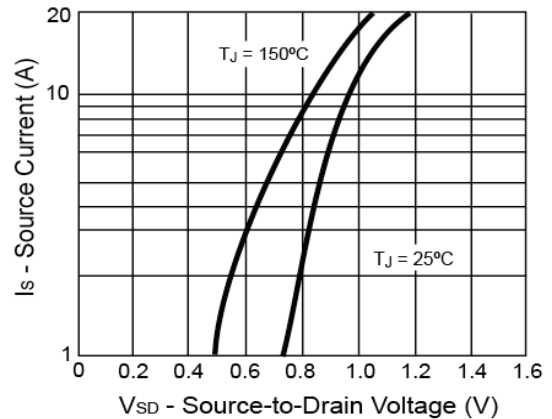
Gate Charge



On-Resistance vs. Junction Temperature



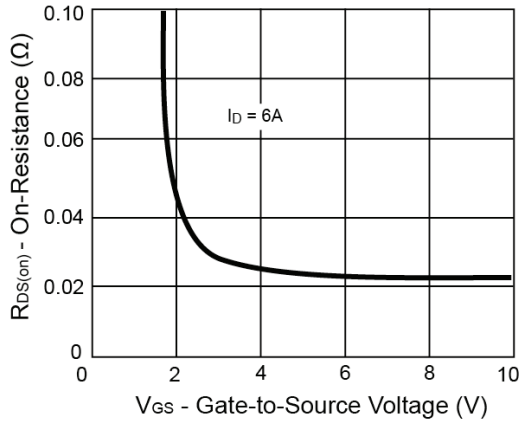
Source-Drain Diode Forward Voltage



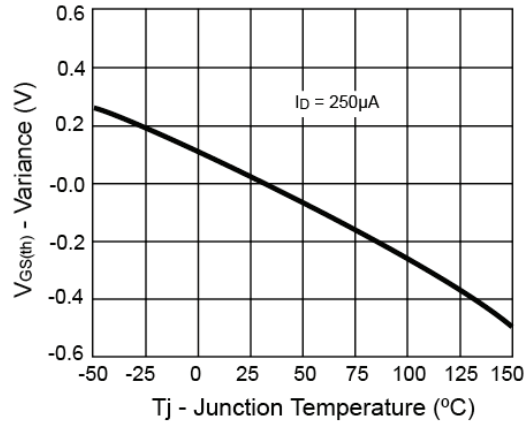
Dual N-channel MOSFET

2KK7103

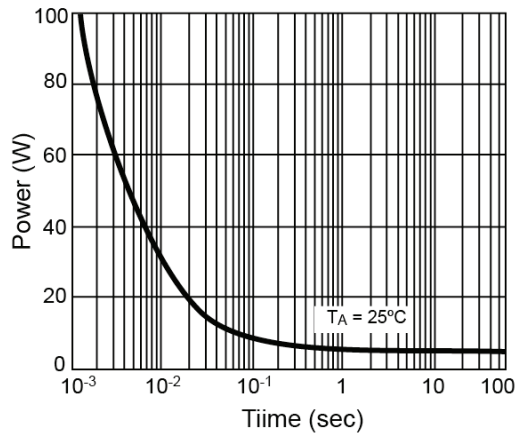
On-Resistance vs. Gate-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

